## CHIPS and Science Act: An Overview

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## **CHIPS Act Summary: appropriated funds**

#### \$50 billion allocated over 5 years for a CHIPS for America Fund

- Implement the Commerce Department <u>semiconductor incentive program</u> to develop domestic manufacturing capability
- R&D and workforce development programs (authorized by FY21 NDAA Sec. 9902 & 9906).
- Specific application guidance for the CHIPS for America program, will be released by **early February 2023**.

#### \$2 billion for a CHIPS for America Defense Fund:

• Funds the <u>Microelectronics Commons</u>, a national network for onshore, university-based prototyping, lab-to-fab transition of semiconductor technologies—including DoD-unique applications—and semiconductor workforce training.

## **CHIPS Act Summary: appropriated funds**

#### \$500 million CHIPS for America International Technology Security and Innovation Fund

 Allocated over 5 years to the Department of State for coordination with foreign government partners to support international information and communications technology security and semiconductor supply chain activities (in coordination with the U.S. Agency for International Development, the Export-Import Bank, and the U.S. International Development Finance Corporation)

#### \$200 million for a CHIPS for America Workforce and Education Fund

• Funding over five years for the National Science Foundation to promote growth of the semiconductor workforce, which faces the need to add 90,000 workers by 2025.

## Semiconductor Incentive Program

\$39 billion allocated over 5 years; up to \$6 billion may fund direct loans and loan guarantees.

- \$19 billion in FY22
- \$5 billion each year, FY23 through FY26

#### Criteria

- 1. Program includes upstream suppliers of semiconductor manufacturing equipment and materials.
- 2. Ensures consideration of a broad range of semiconductors.
- 3. Includes \$2 billion in financial incentives for manufacturing of mature technology nodes, with priority for critical manufacturing industries, such as the automotive industry.
- 4. Entities must have plans in place to identify and mitigate supply chain security risk.
- 5. Prohibits recipients of incentive funds from expanding or building new manufacturing capacity for certain advanced semiconductors in specific countries for 10 years.

## **Research and Development**

#### National Semiconductor Technology Center ("NSTC")

 PPP: Centrally operated, in-house research, engineering, and program capabilities combined with a network of directly funded and affiliated entities. FY22: \$2 billion

#### **National Advanced Packaging Manufacturing Program**

Pilot packaging facility. FY22: \$2.5 billion

#### **Creation of up to 3 Manufacturing USA Institutes**

PPP/consortia. FY22: \$500 million

#### **Metrology research at NIST**

FY22: \$500 million

**National** Semiconductor **Technology Center** National Advanced Metrology R&D Packaging (NIST) Manufacturing Program Manufacturing USA institute(s)

\$11B total investment over five years

National Institute of Standards and Technology | U.S. Department of Commerce

## **Metrology Research**

## NIST Metrology R&D Director To be named late February

Grand challenges developed through industry stakeholder meetings

https://nvlpubs.nist.gov/nistpubs/CHIPS/ NIST.CHIPS.1000.pdf August 2022

#### **Metrology Grand Challenges**

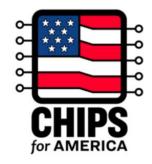
- 1 Metrology for materials purity and properties
- Future microelectronics manufacturing
- Advanced packaging
- Security of devices across the supply chain
- Modeling and simulating semiconductor materials, designs and components
- (6) Improve the manufacturing process
- 7 Standardize new materials, processes and equipment

## **Advanced Manufacturing Investment Credit**

## Creates a 25 percent investment tax credit for investments in semiconductor manufacturing

- Includes incentives for the manufacturing of the specialized tooling equipment required in the semiconductor manufacturing process.
- Credit can be used in conjunction with CHIPS funding opportunities.
- The credit is provided for property which is placed in service after December 31, 2022, and for which construction begins before January 1, 2027.
- Taxpayers may elect to treat the credit as a payment against tax ("direct pay").

## **Key Resource: CHIPS.GOV**



**Implementation Strategy** 

Resources

Webinars

**News & Releases** 

**Industrial Advisory** 

Committee

Current CHIPS Job

**Openings** 



#### A Message from the Secretary of Commerce



The U.S. Department of Commerce is proud to announce the launch of CHIPS.gov



- Considering applying to the CHIPS for America funding opportunity? Prepare to apply by obtaining a <u>SAM.gov</u> registration and Unique Entity Identifier (UEI) number as soon as possible.
- The CHIPS Research and Development Office has published an <u>Update to the Community further describing</u> the National Semiconductor Technology Center.

## **CHIPS for America Defense fund**

#### **Microelectronics Commons**

- \$2 billion over 5 years to reduce barriers to innovation and enhance infrastructure.
- Establish "Lab-to-Fab" testing and prototyping hubs.
- Strengthen microelectronics education pipeline at academic institutions.
- Expect about 10 hub nodes and two core nodes to create the microelectronics commons.



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#### Hubs

A network of regional entities with lab prototyping capabilities and sources of microelectronics talent for onshore, lab-to-fab transition of semiconductor technologies while ensuring workforce training.

#### Hubs:

- Have the flexibility to bring in members from any region to be successful in their lab-to-fab efforts.
- Connect researchers and designers to prototyping capabilities targeted to strengths in the Hub's technical topic areas.
- Will be centers of expertise for one or more of the six critical technology areas.

#### **Microelectronics Commons**



#### <u>Goal</u>

To connect regional organizations through the Hub to accelerate lab-to-fab prototyping based on proximity and to strengthen local economies through a workforce that supports those regions.

#### Cores

Fabs/foundries that have scalable capacity beyond what the regional hubs can provide.

#### Cores serve to:

- Further complement and amplify the work of the regional hubs; for example, ≥200 mm wafer fab for Silicon CMOScompatible technologies and ≥100 mm wafer fab for compound semiconductors.
- Engage with commercial fabs and align them better to commercial processes to facilitate transition to commercial and defense companies.
- Provide access to repeatable processes, back-end manufacturing/integration and full flow-fabrication.



## **Key Resource:**

#### **NSTXL** (National Security Technology Accelerator)

- o <a href="https://nstxl.org/">https://nstxl.org/</a>
- Implemented via "Other Transaction Authority" (OTA)
  - https://s2marts.org/

#### Microelectronics Commons

The Office of the Undersecretary of Defense, Research & Engineering (OUSD(R&E))'s Microelectronics program has a need for domestic prototyping capability to accelerate technology demonstration. Due to the very high complexity of integrated microelectronic systems today, there is an urgent need to establish a network of domestic prototyping facilities to demonstrate, at-scale, the system-level benefits...

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## ...& Science

#### **Authorizes 5-year increases for key science agencies**

|                                                         | Five-Year     | Increase over |
|---------------------------------------------------------|---------------|---------------|
|                                                         | Authorization | Baseline      |
| National Science Foundation (NSF)                       | \$81 billion  | \$36 billion  |
| NSF Tech Directorate                                    | \$20 billion  | \$20 billion  |
| NSF Core Activities                                     | \$61 billion  | \$16 billion  |
| Department of Commerce (DOC)                            | \$11 billion  | \$11 billion  |
| <ul> <li>Regional Technology Hubs</li> </ul>            | \$10 billion  | \$10 billion  |
| RECOMPETE Pilot                                         | \$1 billion   | \$1 billion   |
| National Institute of Standards and Technology          | \$10 billion  | \$5 billion   |
| (NIST)                                                  |               |               |
| NIST Research                                           | \$6.9 billion | \$2.8 billion |
| Manufacturing USA                                       | \$829 million | \$744 million |
| <ul> <li>Manufacturing Extension Partnership</li> </ul> | \$2.3 billion | \$1.5 billion |
| Total                                                   | \$102 billion | \$52 billion  |

DOE Office of Science" increase funding by \$2.6 billion for a total of \$11.1 billion, and grow to \$14.5 billion by FY 2026

## **Export controls & China**

#### **New restrictions on October 2022**

New ECCN 3B090 for specific types of semiconductor manufacturing equipment important to producing advanced node logic semiconductors

End use restriction for any item subject to EAR that supports semiconductor fabrication in China of:

- Logic integrated circuits using a non-planar architecture or with a production technology node of 16/14 nm or less
- NAND memory integrated circuits with 128 layers or more
- DRAM integrated circuits using a production technology node of 18 nm half-pitch or less.

**Expanded Entity List** 





Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification

A Rule by the Industry and Security Bureau on 10/13/2022



## **Upcoming actions?**

#### Harmonized controls with Japan & Netherlands

#### **Executive Order with focus on China**

- Timed after Secretary of State visit to Bejing
- Anticipate additional outbound investment restrictions
  - Quantum
  - $\circ$  Al
  - Semiconductors

#### **Unilateral export controls**

- Quantum controls outside of Wassenaar
  - Error correction algorithms / software
  - End use / application



## **Continued Advocacy**

#### **Congressional Visits Day (CVD)**

Washington, DC

Training: February 28, 2023 (afternoon)

Hill Day: March 1, 2023

#### **SPIE Industry Summit**

Washington, DC Wed Sept 27,2023

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# SPIE.

The international society for optics and photonics